What is claimed is:

1. A method for interconnecting first and second integrated circuits, wherein the first integrated circuit is formed on a working surface of a first semiconductor substrate, the method comprising:

forming at least one high aspect ratio hole through the first semiconductor substrate;

lining the high aspect ratio hole with a material having a high reflectivity for light to form an optical waveguide; and

coupling the first integrated circuit to the second integrated circuit through the optical waveguide.

2. The method of claim 1, and further comprising forming the second integrated circuit on a second surface, opposite the working surface of the first semiconductor substrate.

3. The method of claim 1, and further comprising:

forming the second integrated circuit in a working surface of a second semiconductor substrate; and

bonding the first and second semiconductor substrates together such that the first and second integrated circuits are coupled together through the optical waveguide in the first semiconductor substrate.

4. The method of claim 3, wherein bonding the first and second semiconductor substrates together comprises bonding surfaces of the first and second semiconductor substrates that are opposite the working surfaces of the first and second semiconductor substrates.

5. The method of claim 3, wherein bonding the first and second semiconductor substrates together comprises bonding a working surface of the second semiconductor substrate with a surface of the first semiconductor substrate that is opposite the working surface of the first semiconductor substrate.

6. The method of claim 1, wherein forming at least one high aspect ratio hole comprises:

forming etch pits at selected locations in the first surface of the semiconductor substrate; and

performing an anodic etch of the first semiconductor substrate such that high aspect ratio holes are formed through the first semiconductor substrate at the location of the etch pits.

7. The method of claim 1, wherein coupling the first integrated circuit to the second integrated circuit comprises forming optical transmitters and receivers on opposite ends of the optical waveguide so as to transmit signals between the first and second integrated circuits.

8. The method of claim 7, wherein forming an optical transmitter comprises forming a gallium arsenide optical transmitter that is bonded to a surface of the first semiconductor substrate and forming an optical receiver comprises forming a silicon photodiode detector at an opposite end of the optical waveguide.

9. The method of claim 1, wherein lining the high aspect ratio hole comprises lining the high aspect ratio hole with a layer of tungsten and a layer of aluminum.

10. The method of claim 9, wherein the tungsten layer is formed using a silicon reduction process and a silane reduction process.

11. The method of claim 1, wherein lining the high aspect ratio hole comprises forming a layer of aluminum material.

12. The method of claim 11, wherein forming the layer of aluminum material comprises forming a layer of aluminum material with a thickness of approximately 300 angstroms.

13. The method of claim 1, wherein lining the high aspect ratio holes comprises leaving an opening extending through the semiconductor substrate with a cross-sectional diameter of at least three times the cut-off diameter.

14. An electronic system, comprising:

at least one semiconductor wafer;

a number of integrated circuits with at least one integrated circuit formed on the at least one semiconductor wafer;

the at least one semiconductor wafer including at least one optical waveguide formed in a high aspect ratio hole that extends through the thickness of the at least one semiconductor wafer; and

at least one optical transmitter and at least one optical receiver associated with the at least one optical waveguide that transmit optical signals between selected integrated circuits of the electronic system.

15. The electronic system of claim 14, wherein the number of integrated circuits includes a microprocessor and a memory device.

16. The electronic system of claim 14, wherein the at least one optical waveguide comprises at least one optical waveguide that is formed by an anodic etch that creates at least one high aspect ratio hole through the semiconductor wafer that is lined with a highly reflective material.

17. The electronic system of claim 14, wherein the at least one optical waveguide includes a metallic mirror that lines an inner surface of the high aspect ratio hole.

18. The electronic system of claim 17, wherein the metallic mirror includes a layer of tungsten formed on the inner surface of the high aspect ratio hole and a layer of aluminum formed outwardly from the layer of tungsten.

19. The electronic system of claim 17, wherein the tungsten layer is formed using a silicon reduction process and a silane reduction process.

20. The electronic system of claim 14, wherein the at least one optical waveguide has a cross-sectional diameter of at least three times the cut-off diameter.

21. The electronic system of claim 14, wherein the at least one optical waveguide comprises a layer of aluminum material that lines the high aspect ratio holes.

22. The electronic system of claim 21, wherein the layer of aluminum material has a thickness of approximately 300 angstroms.

23. An integrated circuit, comprising:

a functional circuit formed on a wafer;

a number of optical waveguides formed in high aspect ratio holes that extend through the wafer; and

wherein the optical waveguides include a highly reflective material that is deposited so as to line an inner surface of the high aspect ratio holes.

24. The integrated circuit of claim 23, wherein the number of optical waveguides comprises optical waveguides that are formed by an anodic etch that creates high aspect

ratio holes through the semiconductor wafer that are lined with a highly reflective material.

25. The integrated circuit of claim 23, wherein each optical waveguide includes a metallic mirror that lines an inner surface of the high aspect ratio hole.

26. The integrated circuit of claim 25, wherein the metallic mirror includes a layer of tungsten formed on the inner surface of the high aspect ratio hole and a layer of aluminum formed outwardly from the layer of tungsten.

27. The integrated circuit of claim 26, wherein the tungsten layer is formed using a silicon reduction process and a silane reduction process.

28. The integrated circuit of claim 23, wherein the optical waveguides have a cross-sectional diameter of at least three times the cut-off diameter.

29. The integrated circuit of claim 23, wherein the optical waveguides comprise a layer of aluminum material that lines the high aspect ratio holes.

30. The integrated circuit of claim 29, wherein the layer of aluminum material has a thickness of approximately 100 angstroms.

31. A method for forming an integrated circuit in a semiconductor wafer with an optical waveguide that extends through the semiconductor wafer, the method comprising:

forming a functional circuit in a first surface of the semiconductor wafer;

forming a number of etch pits in the first surface of the semiconductor wafer at selected locations in the functional circuit;

performing an anodic etch of the semiconductor wafer such that high aspect ratio holes are formed through the semiconductor wafer from the first surface to a second, opposite surface;

forming a highly reflective layer of material on an inner surface of the high aspect ratio holes such that the holes have an opening extending through the semiconductor wafer with a diameter that is at least three times the cut-off diameter; and

selectively coupling the optical fiber to the functional circuit.

32. The method of claim 31, wherein forming a highly reflective layer includes forming a metallic mirror that lines an inner surface of the high aspect ratio hole.

33. The method of claim 32, wherein forming the metallic mirror includes forming a layer of tungsten on the inner surface of the high aspect ratio hole and forming a layer of aluminum outwardly from the layer of tungsten.

34. The method of claim 33, wherein forming the tungsten layer includes using a silicon reduction process and a silane reduction process.

35. The method of claim 31, wherein forming the highly reflective layer includes lining the high aspect ratio holes with a layer of aluminum material.

36. The method of claim 35, wherein lining the high aspect ratio holes with the layer of aluminum material includes lining the high aspect ratio holes with a layer of aluminum that has a thickness of approximately 300 angstroms.

37. A method for forming an optical waveguide through a semiconductor substrate, the method comprising:

forming at least one high aspect ratio hole through the semiconductor substrate that passes through the semiconductor substrate from a first working surface to a surface opposite the first working surface; and

lining the high aspect ratio hole with a material having a high reflectivity for light.

38. The method of claim 37, wherein forming the at least one high aspect ratio hole comprises etching high aspect ratio holes in the semiconductor substrate using an anodic etch.

39. The method of claim 38, and further comprising forming etch pits in the working surface of the semiconductor substrate prior to the anodic etch such that the at least one high aspect ratio hole is formed at the location of the etch pits.

40. The method of claim 37, wherein lining the high aspect ratio hole comprises lining the high aspect ratio hole with a layer of tungsten and a layer of aluminum.

41. The method of claim 40, wherein the tungsten layer is formed using a silicon reduction process and a silane reduction process.

42. The method of claim 37, wherein lining the high aspect ratio hole comprises forming a layer of aluminum material.

43. The method of claim 42, wherein forming the layer of aluminum material comprises forming a layer of aluminum material with a thickness of approximately 300 angstroms.

44. The method of claim 37, wherein lining the high aspect ratio holes comprises leaving an opening extending through the semiconductor substrate with a cross-sectional diameter of at least three times the cut-off diameter.

add B1

Add D2